**Committee**

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| **Steering Committee** | |
| **Prasad Mantri** | Principal Engineer, Microelectronics group, Oracle Systems group |
| **Navin Bishnoi** | Deputy Director, ASIC Product Development, GLOBALFOUNDRIES |
| **Thryambak Chandilya** | Applications Engineering Manager - DFT, Mentor Graphics, India |
| **Venkata Rangam Totakura** | Design Engineering Director, Cypress Semiconductor Technologies |
| **Nagesh Tamarapalli** | Fellow, AMD India Design Center |
| **Jyotirmoy Saikia** | Senior Staff R&D Engineer, Test R&D, Synopsys |
| **Anurag Gupta** | Director Engineering, Mobile SoC development, LG Soft India |
| **Manu Lakshmanan** | Principal Application Engineer, Cadence Design System, India |
| **Prof Virendra Singh** | Professor, IIT Mumbai |
| **Prakash Narayanan** | Technical Lead, Texas Instruments |
| **Prof Sivanantham S** | Professor, VIT University |

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| **Yervant Zorian** | (IEEE Fellow) TTTC President |
| **Rohit Kapoor** | (IEEE fellow) TTTC 2nd Vice Chair |
| **Souvik Mahapatra** | (IEEE Fellow) IIT Mumbai |
| **Scott Davidson** | ITC USA liaison |

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**Krishna,**

**Tutorials Co-Chairs**

**Venkata Rangam Totakura**, Cypress Semiconductor Technologies

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Vikram Kuralla, Invecas

Venue:

**Park Plaza Bangalore**  
Outer Ring Rd, Marathahalli Village,   
Marathahalli, Bengaluru, Karnataka 560037

**Profile of Organizing Team**

**Prasad Mantri**

*Prasad Mantri is Principal Engineer at the Microelectronics group at Oracle Systems group. He is involved in Design for Test, Microprocessor Test strategy, Test data volume and test time enhancement, Silicon yield analysis and yield debug, System failure analysis and debug as well as reliability and system product quality. He has worked at Sun Microsystem and Oracle Corporation for the past 13 years working on all their microprocessor designs. Before that, he has worked at Synopsys Inc, SGI, Micron and Silicon access. He has multiple papers and patents in logic and memory test. He has contributed to International Test Conference as a reviewer. He was on the organizing committee of ATE Vision 2020 conference. He has contributed to the ITRS Design and Test roadmap for multiple years as well as presented at the 3D IC design and test workshop organized by Sematec. He is a senior member of the IEEE and has contributed as a volunteer and is working on white papers on IEEE Internet Initiative.  He has M Tech from IIT Madras*

**Navin Bishnoi (Deputy Director, GLOBALFOUNDRIES)**

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*Navin is Deputy Director, ASIC Product Development at GLOBALFOUNDRIES and leads the definition & development of Methodology and Design for ASIC. He is responsible to drive the Global strategy and roadmap for tools, methodology, and architecture in the area of DFT/Test and Low Power. Prior to this, he was with IBM EDA group, leading the development of tools and methodology for DFT, Physical Implementation, and Sign-off flows. He has worked with Freescale, Cadence, and TI for automotive, consumer and custom ASIC designs. He had received his Bachelor’s degree in Electronics and Communication from NIT Surathkal in 1998. He has extensive experience in the field of ASIC designs and required tools/methodology and has been an active member in EDA standards, conferences and review committees. He is Industry Forum Chair for VLSID 2017 and Program Committee Member for Automotive and Reliability Test Workshop @ ITC 2016.*

**Thryambak Chandilya**

Thryambak is the Applications Engineering Manager for DFT at Mentor Graphics, India and leads the field applications and customer support teams at Mentor. He has 16 years of experience in Design-for-Test, and prior to his current role at Mentor Graphics, he was with the Test Development group at Altera Corporation in San Jose focussing on designing DFT structures to test the FPGA fabric. He is responsible for driving new flows and methodologies across Mentor’s DFT product line at customers in the India and South East Asia region. He also works with the R&D team at Mentor to define new flows and methodologies that would improve productivity and quality of test across a wide variety of designs and applications. He has a Master’s degree in Electrical and Electronics Engineering from the University of Florida in Gainesville.

**Venkata Rangam Totakura (***Design Engineering Director, Cypress Semiconductor Technologies)*

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*Venkata is Design Engineering Director at Cypress Semiconductor Technologies. He is responsible for Chip Integration Center (CIC),  implements Synthesis to GDS flow activities for various ASIC products of different Business Units such as Memory, Programmable SoC, Data Communication, and Automotive. He is New Product Development team member and responsible to develop and drive common ASIC implementation methodology across Cypress.  He is DFT CoE (Centre of Excellence) quorum member and DFT-QA review board member at Cypress. He has Masters degree in VLSI CAD. He has 16 years of work experience in VLSI industry, worked for Mentor Graphics, Infineon and NXP organizations intensively into DFT domain. He authored/co-authored 10 papers in DFT and low power domains.He has an extensive experience in the field of ASIC design, implementation and successfully completed multiple Tapeouts in various technology nodes. He has been an active member in EDA standards, conferences and review committees.*

**Nagesh Tamarapalli**

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*Nagesh is an AMD Fellow with AMD India Design Center in Bangalore, India, where he leads a team engaged in high-quality manufacturing test for next generation microprocessors. The team’s mandate spans the entire life cycle of DFT including architecture, implementation, verification, manufacturing test development, silicon bring up and diagnosis. Prior to AMD, he was with Mentor Graphics DFT group where he worked on logic BIST, test compression, and diagnosis tools. He has published several papers in leading test conferences and a paper he co-authored at International Test Conference 1999 on logic BIST has been recognized with “Honorable Mention Award”. He is a co-inventor of 18 US patents in the area of testing. He has delivered DFT seminars at several venues including multiple VLSI Design Conference, ISQED 2007 and DAC 2008. He holds B.Tech. In ECE from REC Warangal, M.Tech. in Electrical Engineering from Indian Institute of Technology, Kharagpur, India, and Ph.D. in Electrical Engineering from McGill University, Montreal, Canada.*

**Jyotirmoy Saikia**

*Jyotirmoy is a Senior Staff R&D Engineer in Test R&D group of Synopsys. He leads the DFTMAX Ultra ATPG R&D there. Jyotirmoy has 12 years of work experience in Test. Jyotirmoy holds 5 issued US Patents in Test Compression area. He is also co-inventor in a few more US patent applications. Jyotirmoy received his master's degree in Computer Science and Engineering from Indian Institute of Technology Kanpur. He is a Senior Member of IEEE and a Senior Member of ACM.*

**Anurag Gupta**

*Anurag is Director Engineering, Mobile SoC development in LG Soft India and responsible for all SoC technical activities and related operations. Prior to LG, he has worked in multiple semiconductor domains and leadership roles in last 18+ years in growing business units of leading technology companies (Freescale Automotive, TI Wireless). He has held chair position of patent review committee in his previous organization (Freescale India) and has been elected for MMTS (in Freescale) and MGTS (in TI) titles.*

**Manu Lakshmanan (**Principal Application Engineer at Cadence Design System, India)



Manu is a principal Application Engineer at Cadence Design System, India and has 16 years of work experience in VLSI field. Prior to his current role at Cadence India, he was with Cadence Design System services group based out of Cary, North Carolina USA where he was involved in coming up with DFT architecture and implementation on various customer designs, he was also involved in top level Synthesis and STA. In his current role, he is responsible for delivering new DFT methodology and flows across existing and new customers. He interacts closely with Cadence R&D to improve tool quality and come up with new methodologies that will help customer productivity and quality of results.

**Krishna Rajan** (Director, Hardware Engineering, Nvidia Graphics Pvt Ltd, Bangalore)



**Prakash Narayanan (Technical Lead, Texas Instruments)**

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**Virendra Singh**

**Scott Davidson**

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*Dr. Scott Davidson is Marketing Chair of ITC, and has been a member of the ITC Steering Committee since 2002, serving as Program Chair in 2004 and General Chair in 2006. He has been involved in test since 1980 at Bell Labs, Intel, Sun Microsystems and Oracle, which he retired from in July 2016. Besides ITC he has been program chair of five workshops, several of which he was a co-founder of. He is currently on the Editorial Board of IEEE Design & Test, and has run the Last Byte column there for nearly 20 years.*

**Dr Yervant Zorian**

*Dr. Yervant Zorian is a Chief Architect and Fellow at Synopsys, as well as President of Synopsys Armenia. Formerly, he was Vice President and Chief Scientist of Virage Logic, Chief Technologist at LogicVision, and a Distinguished Member of Technical Staff AT&T Bell Laboratories. He is currently the President of IEEE Test Technology Technical Council (TTTC), the founder and chair of the IEEE 1500 Standardization Working Group, the Editor-in-Chief Emeritus of the IEEE Design and Test of Computers and an Adjunct Professor at University of British Columbia. He served on the Board of Governors of Computer Society and CEDA, was the Vice President of IEEE Computer Society, and the General Chair of the 50th Design Automation Conference (DAC) and several other symposia and workshops.*

*Dr. Zorian holds 35 US patents, has authored four books, published over 350 refereed papers and received numerous best paper awards. A Fellow of the IEEE since 1999, Dr. Zorian was the 2005 recipient of the prestigious Industrial Pioneer Award for his contribution to BIST, and the 2006 recipient of the IEEE Hans Karlsson Award for diplomacy. He received the IEEE Distinguished Services Award for leading the TTTC, the IEEE Meritorious Award for outstanding contributions to EDA, and in 2014, the Republic of Armenia's National Medal of Science.*

*He received an MS degree in Computer Engineering from University of Southern California, a PhD in Electrical Engineering from McGill University, and an MBA from Wharton School of Business, University of Pennsylvania.*

**Souvik Mahapatra**

*Souvik received his PhD in Electrical Engineering from IIT Bombay, Mumbai, India in 1999. During 2000-01, he was with Bell Labs, Lucent Technologies, Murray Hill, NJ, USA. Since 2002 he is with the Department of Electrical Engineering at IIT Bombay and currently holds the position of full professor. His current research interests are in the area of CMOS logic gate stacks – scaling and reliability. He has published more than 150 papers in peer reviewed journals and conferences, delivered invited talks and tutorials in major international conferences including at the IEEE IEDM and IEEE IRPS, and served as a committee member and session chair in several IEEE conferences. He is a fellow of the Indian National Academy of Engineering, Fellow of IEEE and a distinguished lecturer of IEEE EDS*.

**Rohit Kapur**

*Rohit is a Fellow in Synopsys. A recognized authority in Test, he holds 25 patents and over a hundred publications.*

*Rohit has made contributions to leading Synopsys products including DFTMAX, DFTMAX Ultra, and TetraMAX. His most notable innovations have been in pattern compression and in test vector quality with slack-based transition testing.*

*Rohit received his PhD in Computer Engineering from the University of Texas in 1992.  Rohit is IEEE Fellow and TTTC 2nd Vice Chair. He was the group chair for the IEEE Core Test Language (CTL) standard. He is also in the editorial board of the Computer magazine.*